Amendments to the Specification

Please amend the following paragraphs of the specification:

[0015] Each of the buffered signals (including the input signals and the processed signals) is assigned a global identification code. One or more of the buffered signals are converted into a packetized signal by a packetized signal output stage in each input processor. Each packetized signal contains a series of packets. Each packet contains a part of the data from the buffered signal along with the global identification code of the buffered signal. An input processor may have more than one packetized signal output stages to produce more than one packetized signal.

[0033] The input processor 104 may also contain a bank of input signal analyzers (not shown). The input signal analyzers may be dynamically or statically coupled to an input port in the same manner as A/D converter 150. For example if the input signal is a video signal, an input signal analyzer may extract performance and signal content metrics from or about the input signal such as blackness of the signal, the amount of motion within the signal, bit or formatting errors in the signal. The metadata produced by the ~~the~~ data analyzer is stored in a data buffer and is considered and treated as a processed signal that can be packetized and coupled to the output processor over a communication link.

[0042] The data compressors 164 may include horizontal or vertical line filters that produce a processed video data signal comprising a portion of the video data from a video input data signal. For example, a horizontal line filter may be configured to horizontally compress a 640 x 400 pixel video signal into a 320 x 400 pixel video signal by discarding every other pixel in each line of the video signal. A vertical line filter may be configured to compress a 640 x 400 pixel video signal into a 640 x 200 pixel video signal by discarding every other line in the video signal. A horizontal/vertical line filter

may be configured to compress a 640 x 400 pixel video signal into a 160 x 100 pixel video signal by discarding three of every four lines of the video signal and discarding three of every four pixels in each line that is retained.

[0058] In the present example, the input processor local controller 140 configures the input processor 104 as follows:

i. Store input signal 110a in data buffer 124a. Assign global identification code G101 to the stored signal.

ii. Store input signal 110b in data buffer 124b. Assign global identification code G102 to the stored signal.

iii. Store input signal 110d in data buffer 124c. Assign global identification code G103 to the stored signal.

iv. Couple an A/D converter 150 between input port ~~108e~~123e at which input signal 110e is received to produce a digital version 110e' of input signal 110e. Store digital signal 110e' in data buffer 124e. Assign global identification code G104 to the stored signal.

v. Couple video scaler 160a to memory system 122 to retrieve signal G101 and produce a scaled version of 400 x 300 pixel scaled version of signal G101. The scaled version is stored in data buffer 124f and is assigned global identification code G105.

vi. Couple video scaler 160b to memory system 122 to retrieve signal G101 and produce a 610 x 460 pixel scaled version of signal G101. The scaled version is stored in data buffer 124g and is assigned global identification code G106.

vii. Couple video scaler 160c to memory system 122 to retrieve signal G102 and produce a 200 x 113 pixel scaled version of signal G102. The scaled version is stored in a memory buffer 124h and is assigned global identification code G107.

viii. Couple video scaler 160d to memory system 122 to retrieve signal G102 and produce an 1140 x 640 pixel scaled version of signal G102. The scaled version is stored in data buffer 124i and is assigned global identification code G108.

ix. Couple video scaler 160e to memory system 122 to retrieve signal G103 and produce a 160 x 120 pixel scaled version of signal G103. The scaled version is stored in data buffer 124j and is assigned global identification code G109.

x. Couple video scaler 160f to memory system 122 to retrieve signal G104 and produce a 560 x 420 pixel scaled version of signal G104. The scaled version is stored in data buffer 124k and is assigned global identification code G110.

xi. Couple a signal analyzer (one of the signal processors 126, as described above) to the memory system 122 to retrieve and analyze signal G102. The signal analyzer produces a video signal with a standard size of 320 x 200 pixels and metadata. The output of the signal analyzer is stored in data buffer 124m and is assigned global identification code G111.

xii. Couple a video scaler 160g to memory system 122 to retrieve signal G111 and produce a 440 x 140 pixel scaled version of signal G111. The scaled version is stored in data buffer 124n and is assigned global identification code G112.

[0086] The output signal generator 212 can generate a variety of digital output signals that may be used directly, or after conversion through a D/A converter 215, by output device 116. The output signal generator 212 may include one or more digital video signal generators, one or more digital audio signal generators or one or more data signal generators or any combination of video, audio and data signal generators. The data signal generators may include TCP/IP signal generators that produce an output

signal 114 suitable for transmission using a communications link to a remote computer system, where the output signal may be decoded and used by a video, audio or data system. Similarly, the data signal ~~generate~~ generator may ~~generator~~ generate signals in any data format.

[0090] To produce the video signals for the example output video monitors 116a (Figure 3) and 116b (Figure 4), the output processor local controller configures the output processor 106 to operate as follows:

i. Packetized signal extractor 206 operates as follows:

a. Extract signal G105 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B201 and store it as an output source signal in data buffer 220a;

b. Extract signal G106 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B202 and store it as an output source signal in data buffer 220b;

c. Extract signal G107 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B203 and store it as an output source signal in data buffer 220c;

d. Extract signal G108 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B204 and store it as an output source signal in data buffer 220d;

e. Extract signal G109 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B205 and store it as an output source signal in data buffer 220e;

f. Extract signal G110 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B206 and store it as an output source signal in data buffer 220f; and

g. Extract signal G112 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B207 and store it as an output source signal in data buffer 220g.

ii. Local signal generator 224 produces a 200 x 150 pixel data and time window as described above. Assign local identification code B208 to this signal and store it as an output source signal in data buffer 220h.

iii. Output signal generator 212 generates two output signals as follows:

a. One output video signal generator 212a extracts local signals B201, B203, B205, B207 and B208 from the corresponding data buffers 220 and produces an output signal 114a.

b. A second output video signal generator 212b extracts local signals B202 B204 and B206 from the corresponding data buffers 220 and produces an output signal 114b.

iv. A D/A converter is coupled between video signal generator 212a and output terminal to convert output signal 114a into [[a]]an ~~digital~~analog output signal, which is then displayed by video monitor 116a.

v. Output signal 114b is coupled directly to output port 214b. Video monitor 116b receives and displays the digital output signal 114b.

[0098] Reference is next made to Figure 9, which illustrates three input processors 304 and two output processors 403. Input processor 304a receives eight input signals from eight sources 108a – 108h and generates two packetized signals 112a and 112b. Input processor 304b receives eight input signals from eight sources 108i – 108p and generates two packetized signals 112c and 112d. Input processor

304c receives eight input signals 108q – 108x and generates one packetized signal 112e. Output processor 403a ~~receive~~receives packetized signals 112a and 112c and produces four output signals 114a – 114d at output terminals 714a – 714d. These output signals may include information from any of the sixteen input signals 108a – 108p. Output processor 403b receives packetized signals 112b, 112d and 112e and produces four output signals 114e – 114h at terminals 714e – 714h. The output signals 114a – 114h may include information from any of the twenty-four input signals 108a – 108x. In each case, each input source is coupled to only one input processor, but may be combined with the other input sources in the output signals.